AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A circuit arrangement for electronic data processing comprising:

at least one non-volatile memory module for storing encrypted data to be protected against unauthorized access;

at least one memory module interface logic circuit in electronic communication with the memory module; said at least one memory module interface circuit being for addressing the memory module, for writing the data to the memory module, or for reading out the data from the memory module;

at least one code Read Only Memory (ROM) module for storing and/or supplying at least one ROM code; and

at least one code ROM module interface logic circuit in electronic communication with the code ROM module for addressing the code ROM module and for reading out the ROM code from the code ROM module,

wherein the at least one ROM code stored in the code ROM module is used to generate at least one key code for encrypting or decrypting data being written to the memory module or data being read from the memory module, said at least one ROM code further being used for decrypting a memory module address coming from a central processing unit (CPU)~~an address of said memory module~~.

2. (Currently Amended) A circuit arrangement as claimed in claim 1, wherein the memory module interface logic circuit comprises at least one en-/decryption logic circuit

- having at least one key address generation unit for generating a ROM key address using a memory module address coming from the CPU and

- having at least one key register.

3. (Previously Presented) A circuit arrangement as claimed in claim 1, wherein the code ROM module interface logic circuit comprises at least one multiplexing unit.

4. (Previously Presented) A circuit arrangement as claimed in claim 1, wherein the memory module takes the form of

at least one erasable programmable read only memory (EPROM),

at least one electrical erasable programmable read only memory (EEPROM) or

at least one Flash memory.

5. (Previously Presented) A microcontroller, in particular an "embedded security controller", comprising at least one circuit arrangement as claimed in claim 1.

6-10. (Canceled)

11. (Withdrawn) A method of retrieving encrypted data from a non-volatile memory for use by a microprocessor, said method comprising:

receiving, by a memory module interface logic circuit, an encrypted address from a central processing unit (CPU);

receiving, by a code ROM module interface logic circuit an address from the CPU;

using the address to read a key code from a code ROM;

providing the key code to the memory module interface logic circuit for decrypting the encrypted address into an unencrypted address;

reading encrypted data from the unencrypted address of said non-volatile memory by the memory module interface logic circuit;

decrypting said encrypted data using the key code, and

providing said decrypted data to said CPU.

12. (Withdrawn) The method of claim 11, wherein receiving the encrypted address and receiving the address are performed in parallel.

13. (Withdrawn) The method of claim 11, wherein the code ROM only stores key codes.

14. (Withdrawn) A method of storing encrypted data into a non-volatile memory, said method comprising:

receiving, by a memory module interface logic circuit, an encrypted address from a central processing unit (CPU);

receiving, by a code ROM module interface logic circuit an address from the CPU;

receiving, by the memory module interface logic circuit, data;

using the address to read a key code from a code ROM;

providing the key code to the memory module interface logic circuit for decrypting the encrypted address into an unencrypted address and for encrypting the data into encrypted data; and

writing, by the memory module interface logic circuit, the encrypted data to the unencrypted address of said non-volatile memory.

15. (Withdrawn) The method of claim 14, wherein said receiving steps are performed in parallel.

16. (Currently Amended) A microcontroller comprising a security controller circuit, said security controller circuit comprising:

a non-volatile memory for storing encrypted data;

a memory module interface logic circuit for reading and writing encrypted data to and from said non-volatile memory;

a code ROM for storing a plurality of key codes; and

a code ROM module interface logic circuit for receiving an address from said microcontroller, for using said address to read a key code from said code ROM, and for providing said key code to said memory module interface logic circuit;

said memory module interface logic circuit being further for receiving an encrypted memory module address from a central processing unit (CPU) and data from said microcontroller, for using said key code to decrypt said encrypted memory module address, for encrypting said data, and for storing said encrypted data in said decrypted memory module address of said non-volatile memory.